the at least one of the pipeline stages including processing circuitry with an active state which is entered when the data received by the at least one of the pipeline stages has a predetermined activation pattern, the predetermined activation pattern corresponding to one of the different standards;

the at least one of the pipeline stages including a state machine having a current state and a previous state; and

wherein the at least one of the pipeline stages is activated upon recognition of the predetermined activation pattern only upon a predetermined transition from the previous state to the current state.

2. The pipeline system of claim 1, wherein the processing circuitry has an inactive state, in which the at least one of the pipeline stages passes data to a following pipeline stage without processing.

3. The pipeline system of claim 1, wherein the sequence of pipeline stages includes at least one spatial decoder stage.

4. The pipeline system of claim 1, wherein the sequence of pipeline stages includes at least one temporal decoder stage.

5.The pipeline system of claim 1, wherein the at least one of the pipeline stages is a spatial decoder stage.